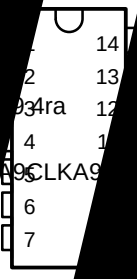
5620C,
AD 8-BIT DIGI G CON

SLAS – REVISED

- **Four 8-Bit Voltage Outpu**
- **5-V Single-Supply Opera**
- **Serial Interface**
- **High-Impedance Referenc**
- **Programmable 1 or 2 Time ge**
- **Simultaneous Update Faci**
- **Internal Power-On Reset**
- **Low-Power Consumption**
- **Half-Buffered Output**

PACKAG
P VIEW)



applications

- **Programmable Voltage Sour**
- **Digitally Controlled Amplifie o**
- **Mobile Communications**
- **Automatic Test Equipment**
- **Process Monitoring and Cont**
- **Signal Synthesis**

description

The TLC5620C and TLC5620I ar tage ou ital-to-an buffered reference inputs (high imp produce tput volta one or two times the reference volta the DAC monoton running from a single supply of 5 V unction corporate conditions.

Digital control of the TLC5620C and T a simpl ee-wire s and easily interfaced to all popular d micr troller de comprises eight bits of data, two DAC b ange b e latter a 1 or times 2 output range. The DAC re buffer allowing written to the device, then all DAC ou simu neously t inputs feature Schmitt triggers for high

The 14-terminal small-outline (D) p digital control o applications. The TLC5620C is charac ion fr m 0°C to for operation from –40°C to 85°C. The TLC5620I do n

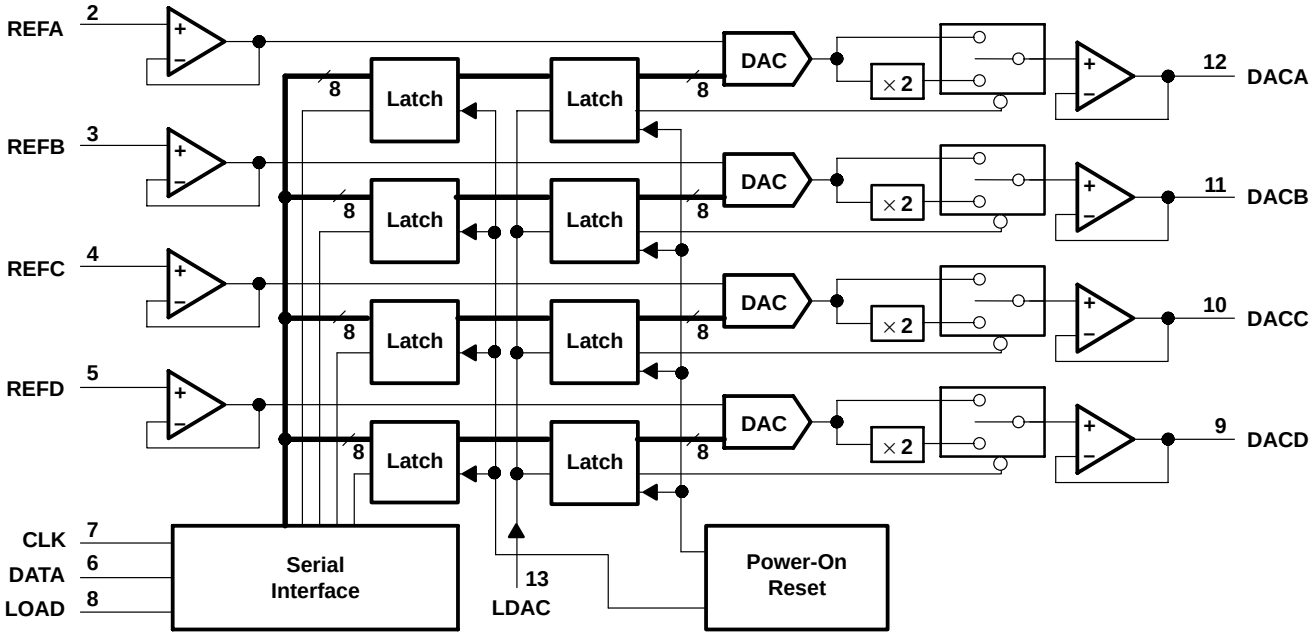
TIONS

	E	
T_A	LIN	PL
0°C to 70°C	C	T
–40°C to 85°C	I	

Please be aware that c availability Texas Instruments rs th eto a

PRODUCTION DATA inform
Products conform to spe
standard warranty. P
testing of all para

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	7	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	1	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When the LDAC signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	8	I	Serial Interface load control. When LDAC is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REFA	2	I	Reference voltage input to DAC A. This voltage defines the output analog range.
REFB	3	I	Reference voltage input to DAC B. This voltage defines the output analog range.
REFC	4	I	Reference voltage input to DAC C. This voltage defines the output analog range.
REFD	5	I	Reference voltage input to DAC D. This voltage defines the output analog range.
V_{DD}	14	I	Positive supply voltage

detailed description

The TLC5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Since the inputs are buffered, the DACs always present a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier that can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is 0 or 1 within the serial control word.

Table 1. Ideal Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered most significant bit (MSB) first. Data transfers using two 8-clock cycle periods are shown in Figures 3 and 4.

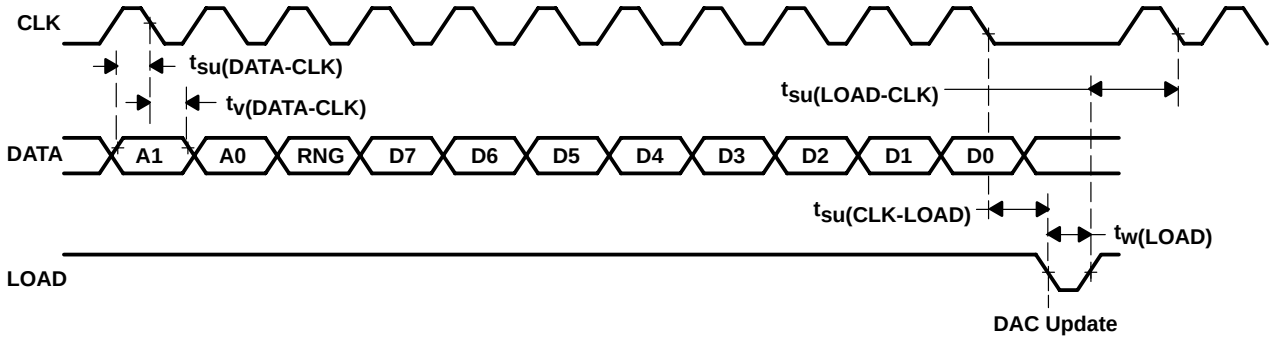
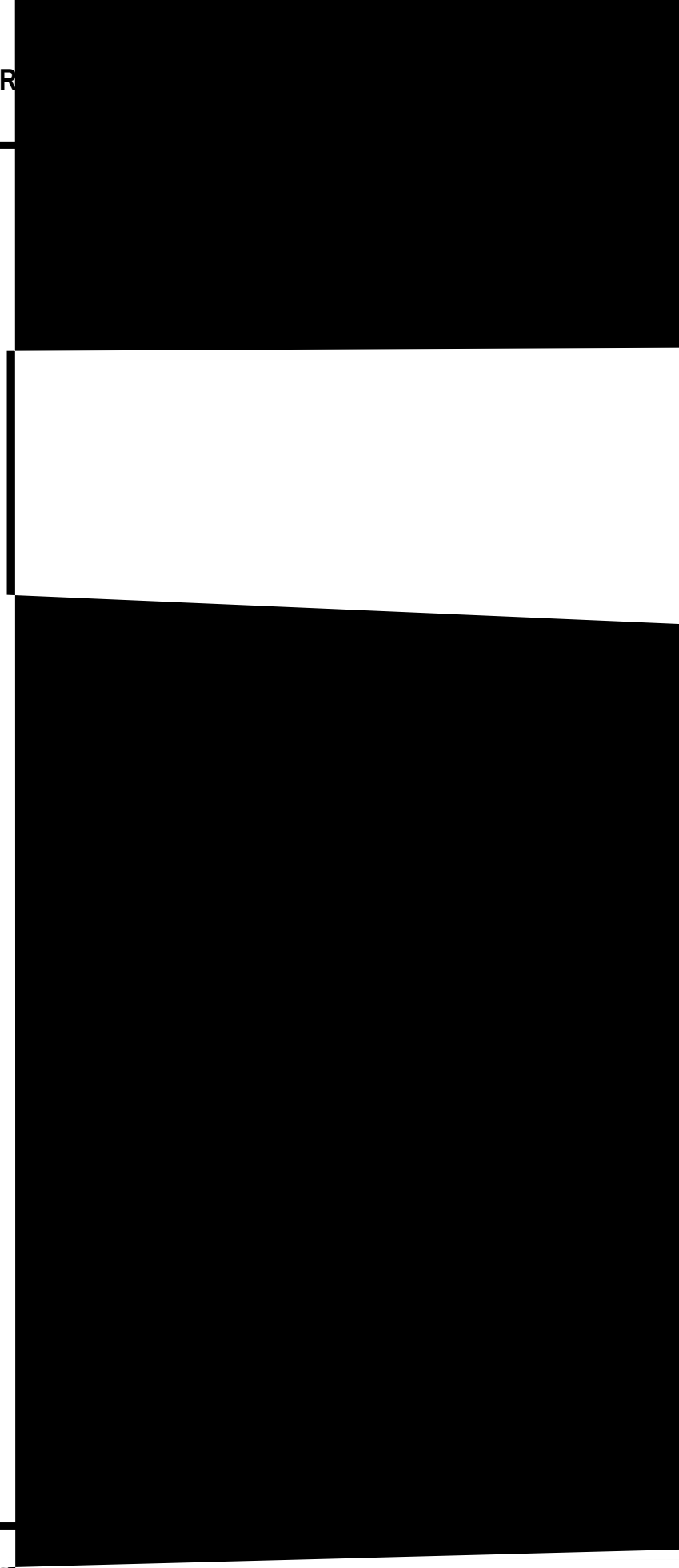
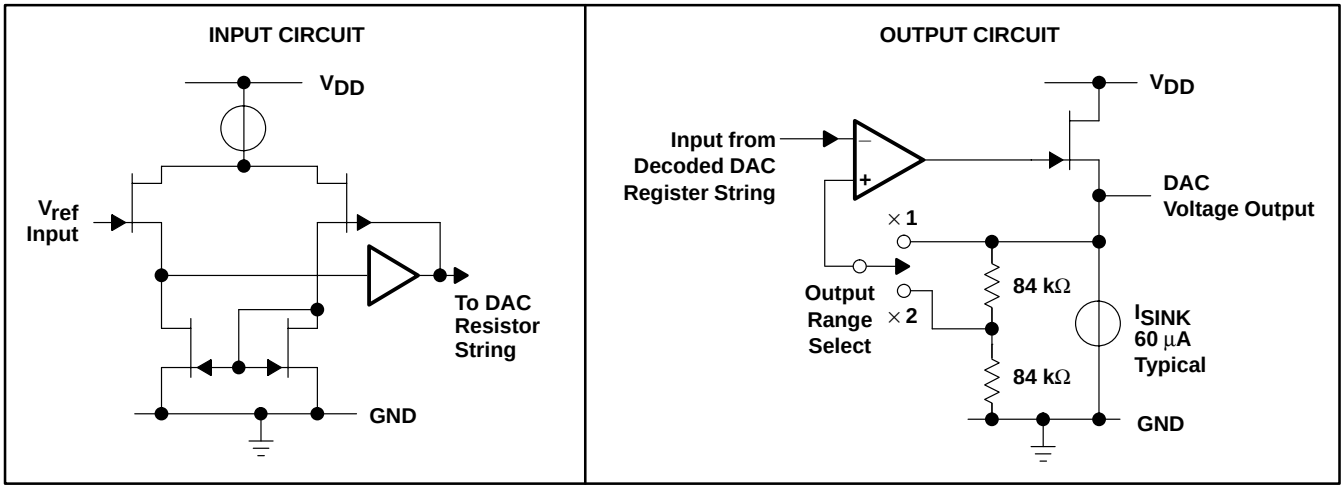


Figure 1. LOAD-Controlled Update (LDAC = Low)



equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) . . . . . 7 V
Digital input voltage range . . . . . GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range, V_{ID} . . . . . GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLC5620C . . . . . 0°C to 70°C
TLC5620I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75		5.25	V
High-level input voltage, V_{IH}		0.8 V_{DD}			V
Low-level input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [A|B|C|D]				V_{DD}–1.5	V
Analog full-scale output voltage, R_L = 10 kΩ			3.5		V
Load resistance, R_L		10			kΩ
Setup time, data input, $t_{su(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Setup time, CLK eleventh falling edge to LOAD, $t_{su(CLK-LOAD)}$ (see Figure 1)		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$ (see Figure 1)		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$ (see Figure 1)		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$ (see Figure 2)		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$ (see Figure 2)		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLC5620C	0		70	°C
	TLC5620I	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT

PARAMETER MEASUREMENT INFORMATION

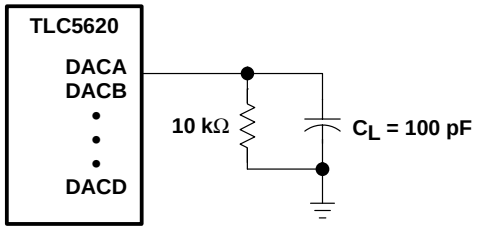


Figure 6. Slew, Settling Time, and Linearity Measurements

TYPICAL CHARACTERISTICS

POSITIVE RISE AND SETTLING TIME

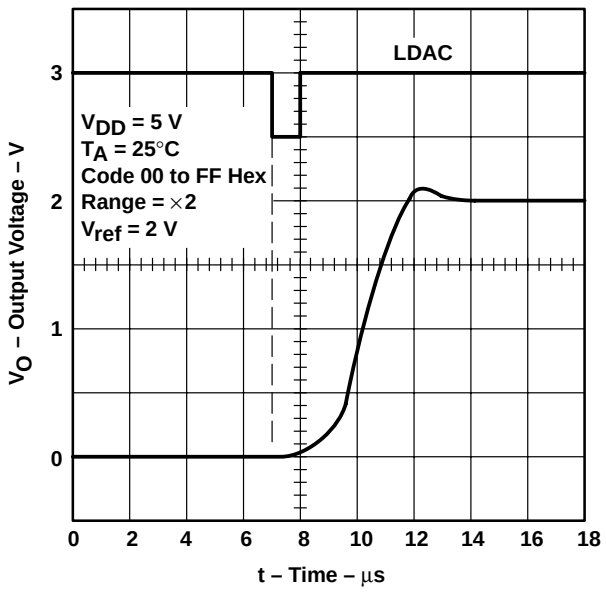


Figure 7

NEGATIVE FALL AND SETTLING TIME

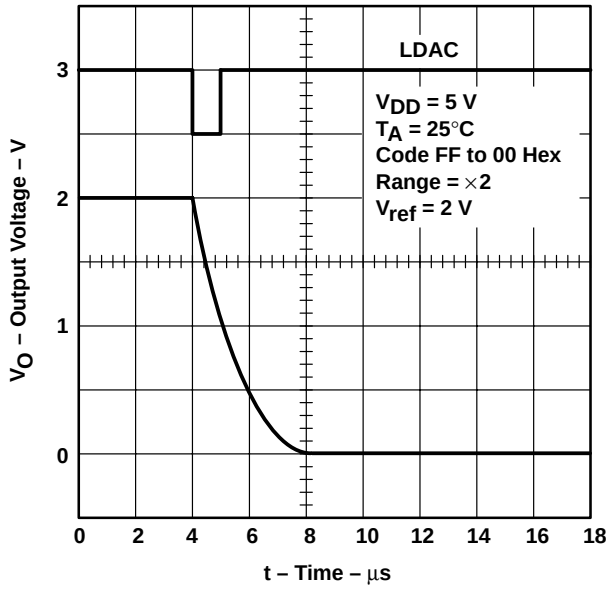


Figure 8

TYPICAL CHARACTERISTICS

DAC OUTPUT VOLTAGE
vs
OUTPUT LOAD

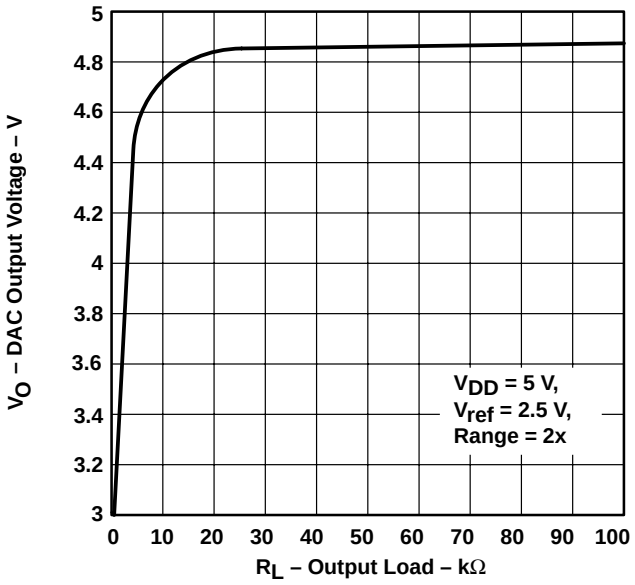


Figure 9

DAC OUTPUT VOLTAGE
vs
OUTPUT LOAD

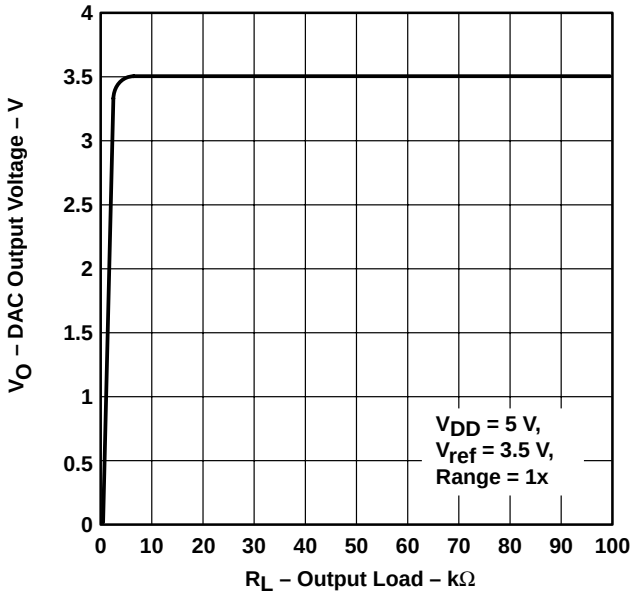


Figure 10

OUTPUT SOURCE CURRENT
vs
OUTPUT VOLTAGE

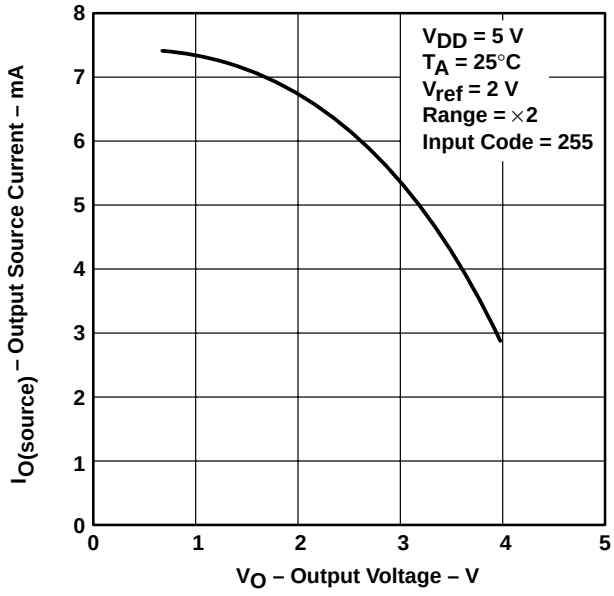


Figure 11

SUPPLY CURRENT
vs
TEMPERATURE

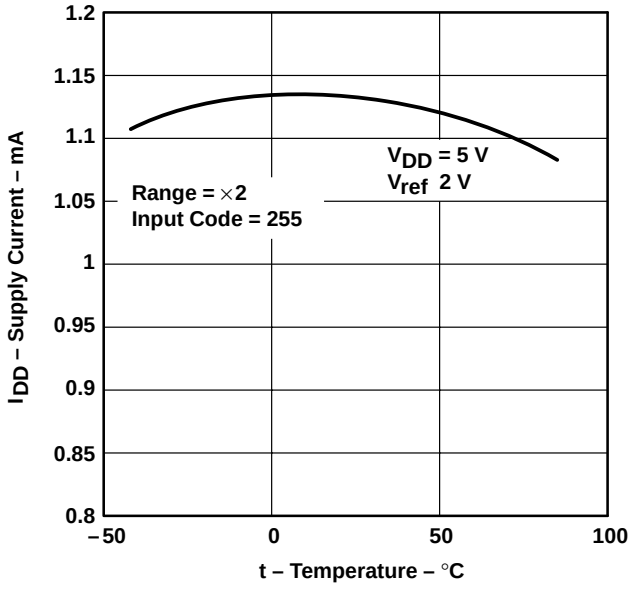


Figure 12

MECHANICAL DATA

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLC5620CD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC5620CDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC5620CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA
TLC5620ID	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC5620IDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC5620IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NA-NA-NA

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for

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Mailing Address: Texas Instruments
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